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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,115	09/10/2003	Sun Hyoung Lee	DAE-0009	3574

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,115	LEE ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,12-18,20* is/are rejected.

7)☒ Claim(s) *6,11 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Response to amendment filed on 5/5/2006
- Amended claims 1- 20 have been submitted for examination
- Amended claims 1- 5,7-10,12-18 and 20 have been rejected
- Claims 6,11 and 19 are objected to.

Claim Rejections - 35 USC § 112

1. In view of the amended claims 3, 8 and 8, filed on 5/5/2006, all rejections under section 35 USC § 112 are withdrawn.

Response to Arguments

2. Applicant's arguments with respect to amended claims 1 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Shau US publication no. 2002/0121886 (Hereinafter Shau).

4. In regard to claim 1, Shau teaches:

- (Currently Amended) An SRAM-compatible memory including a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the DRAM cells interfacing with an external system which does not provided separate timing period for performing a refresh operation for the DRAM cells, comprising:

(Note: FIG. 2 and section [0007] in Shau)

- the memory banks for receiving and storing input data externally provided, memory banks generating bank information signals each indicating whether a corresponding memory bank is subjected to an invalid read-access;

(Note: section [0050] in Shau)

- a parity generator for receiving the input data to generate input parity, the input parity being determined based on the input data and a preset parity value;

(Note: section [0051] in Shau)

- a parity bank for storing the input parity and generating a parity bank information signal indicating whether the parity bank is subjected to the invalid read-access;

(Note: sections [0051] through [0057] in Shau)

- a refresher timer generating a refresh request signal periodically to activate the refresh operation for both the memory banks and the parity bank; and

(Note: section [0061] in Shau)

- a data corrector receiving the bank information signals and the fetched data from the memory banks and generating output data having same value as the input data by correcting data fetched from a memory being subjected to the invalid read-access if a checked parity values different from the preset parity values the checked parity value being obtained being the fetched data provided from the memory banks and parity data fetched from the parity bank.

(Note: [0058] in Shau)

5. In regard to claim 2, Shau teaches:

- (Original) The SRAM-compatible memory according to claim 1, wherein the data corrector comprises:
- a bank data control unit for receiving the. bank information signals and the fetched data to provide bank control data, any of the bank control data corresponding to fetched data provided from any of the memory banks subjected to the invalid read-access has a first logic value;
- a parity data control unit for receiving the parity information signal and the parity data fetched from the parity bank to provide parity control data;

- a discriminating unlit for receiving the bank control data and the parity control data and providing discrimination data having a second logic value contrary to the first logical value if the fetched parity data is different from the input parity; and
- a selecting unlit for selecting the bank control data or the discrimination data in response to the bank information signals to generate the output data.

(Note: Figures 2(e) and 2(f) and section [0058] in Shau)

6. In regard to claim 3, Shau teaches:

- (currently Amended) The SRAM-compatible memory according to claim 2, wherein the parity bank has a substantially same capacity and structure as each of the memory banks.

(Note: Figures 5(a) through 5(d) in Shau)

7. In regard to claim 4, Shau teaches:

- (Original) The SRAM-compatible memory according to claim 2. wherein the memory banks each independently store corresponding one of the input data.

(Note: FIG. 2(a), reference sign (301) in Shau)

8. In regard to claim 5, Shau teaches:

- (Original) The SRAM-compatible memory according to claim 2, wherein each of the memory bank independently perform a read-access operation in response to a read command externally provided.

(Note: FIG. 2(c) in Shau)

9. In regard to claim 7, Shau teaches:

- (Original) The SRAM-compatible memory according to claim 2, wherein: the bank data control unit includes a plurality of first logic devices each performing logic AND option with respect to an inverted signal of corresponding one of the bank information signals and the fetched data provided from corresponding one of the memory bank to generate corresponding one of the bank control data and the parity data control unit includes a second logic device performing logic AND operation with respect to an inverted signal of the parity information signal and the parity data to provide the parity control data.

(Note: FIG. 2(f) in Shau)

10. Claims 8 and 16 are rejected for the same reasons as per claim 3.

11. Claim 9 and 17 are rejected for the same reasons as per claim 4.

12. Claim 10 and 18 are rejected for the same reasons as per claim 5.

13. In regard to claim 12, Shau teaches:

- (Original) The SRAM-compatible memory according to claim 7, wherein the selecting unit includes a plurality of multiplexers each receiving corresponding one of the bank control data from corresponding one of the first logic devices and the discrimination data from the discriminating unlit and selecting the corresponding one of the

bank control data or the discrimination data in response to corresponding one of the bank information signals.

(Note: FIG. 2 in Shau)

14. In regard to claim 13, Shau teaches:

- (Original) The SRAM-compatible memory according to claim 12, wherein the multiplexers each select the discrimination data when the corresponding one of the bank information signals indicates that the fetched data is provided from a memory bank subjected to the invalid read-access.

(Note: FIG. 2 in Shau)

15. In regard to claim 14, Shau teaches:

- (Original) The SRAM-compatible memory According to claim 13, wherein the multiplexers each select the corresponding one of the bank control data when the corresponding one of the bank information signals indicates that the fetched data is valid.

(Note: FIG. 2 and section [0051] in Shau)

16. In regard to claim 15, Shau teaches:

- (Original) The SRAM-compatible memory according to claim 2. wherein the selecting unit includes a plurality of multiplexers for providing one of the discrimination data and the bank control data as the output data in response to the bank information signals.

(Note: FIG. 2 in Shau)

17. Claim 20 is rejected for the same reasons as per claim1.

Allowable Subject Matter

18. Claims 6, 11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

19. In regard to claim 6, the prior Art of record and, in particular Shau, teaches substantially all the limitations in claims 1 and 2.

However, the prior art do not teach, suggest, or otherwise render obvious:

The SRAM-compatible memory according to claim 2, wherein the refresh operation is independently performed with respect to the respective memory banks, and is prevented from being simultaneously performed with respect to two or more memory banks.

As structured in claim 6.

20. Claims 11 and 19 have similar language as in claim 6.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571)-272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

7/12/06

ALBERT DECADY
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